49. The system of claim 40, wherein each driver includes control circuitry configured to generate a third status signal indicative of a particular memory cell coupled to the associated bit line being incompletely programmed.

50. The system of claim 49, wherein the plurality of drivers are configured to generate a fourth status signal indicative of at least one memory cells associated with the plurality of drivers being incompletely programmed.

51. The system of claim 50, the fourth status signal is generated by wired-ORing third status signals from the plurality of drivers.

52. The system of claim 50, wherein the third status signals from the plurality of drivers are each provided to a gate of a respective one of a plurality of pull-down transistors, and wherein the fourth status signal is generated by coupling drains of the pulldown transistors.

53. The system of claim 4, wherein voltages for memory cells not selected for programming are set to approximately zero.--

IN THE DRAWINGS:

Please amend Figs. 4A-4C and 14 as indicated by the redlined revisions. Applicants submit that no new matter has been added.

REMARKS

This is a divisional application of application serial number 09/231,928 filed on January 14, 1999. Claims 1 through 3 have been cancelled. Claims 4 through 53 have been added.